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	SPECIFICATION	■DUTY PANEL DEVELOPMENT CENTEF ☐TFT DEVELOPMENT CENTER ☐LCD PRODUCTS DEVELOPMENT CENTER ❑ IEL PRODUCTION DEPT.

Device specification for Passive Matrix LCD module

Model No.

LM64K103

❑ ICUSTOMER'S APPROVAL

DATE

BY

PRESENTED BY

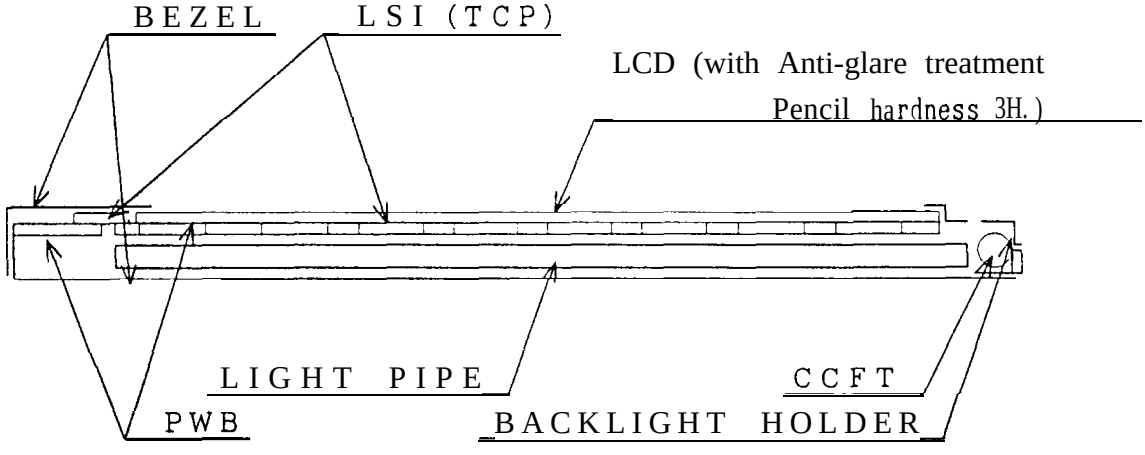
Y. Inoue
Department General Manager
Engineering Department 2
DUTY Panel Development center
LCD GROUP

1. Application

This data sheet is to introduce the specification of LM64K103,Passive Matrix type LCD Module

2. Construction and Outline

Construction:640 X480 dots display unit consisting of an LCD panel, PWB(printed wiring board) with electric components mounted onto,TCP(tape carrier Package) to connect the LCD panel and PWB electrically, and plastic chassis with CCFT backlight and bezels to fix them mechanically.



Outline : See Fig. 10

Connection : See Fig. 10 and Table 6

3. Mechanical Specifications

Table 1

Parameter	Specifications	Module
Outline dimensions	200,5(W) X141 (H) × 7MAX(D)*1*2	mm
Effective viewing Area	151(W) X113,4(H)	mm
Display format	640(W) X480(H) full dot	−
Dot size	0.21X0.21	mm
Dot spacing	0.02	mm
Dot color	Black*3*4	−
Background color	White*3*4	−
Weight	Approx. 260	g

*1 Excluded the mounting tabs.

*2 Excluded the allowance of deformation.

*3 Due to the characteristics of the LC material, the colors vary with environmental temperature.

*4 Positive-type display
Displayed data “H”: Dots ON : Black
Displayed data “L”: Dots OFF: White

4. Absolute Maximum Ratings

4-1 Electrical absolute maximum ratings

Table 2

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply voltage (Logic)	V_{DD}-V_{SS}	0	6.0	V	Ta=25 “C
Supply voltage (LCD drive)	V_{DD}-V_{EE}	0	28,0	V	Ta=25 “C
Input voltage	V_{IN}	0	V_{DD}	V	Ta=25 ℃

4-2 Environmental Conditions

Table 3

Item	Tstg		Topr		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperatuer	-25 'C	+70 "c	o "c	+50 "c	Note 4
Humidity	Note 1		Note 1		No condensation
Vibration	Note 2		Note 2		3 directions (X/Y/2)
Shock	Note 3		Note 3		6 directions (±X±Y±Z)

Note 1) Ta≦40 'C ... ..95 % RH Max

Ta>40 'C .....Absolute humidity shall be less than Ta=40 ℃/95 % RH.

Note 2) These test condition are in accordance with "IEC68-2-6".

Frequency	10 Hz～57 Hz	57 Hz-500 Hz
Vibration level	–	9.8 m/s² (1 G)
Vibration width	0.075 mm	–
Interval	5 Hz～500 Hz-5 Hz/n min	

2 hours for each direction of X/Y/Z (6 hours as total)

Note 3) Accerelation : 490 m/s²

Pulse width : 11 ms

3 times for each direction of ±X／±Y／±Z

Note 4) Care should be taken so that the LCD Module may not be subjected to the temperature out of this specification.

5. Electrical Specifications

5-1 Electrical characteristics

Tabel 4 Ta=25 "C

Parameter	Symbol	Conditions	Min.	TYP.	Max.	Unit
Supply voltage (Logic)	V_{DD}-V_{SS}		2.7	**3.0**	5.5	**v**
Supply voltage (LCD drive)	V_{DD}-V_{EE}	Note 1) Note 2)	18.4	22.0	26.4	**v**
Input signal voltage	V_{IN}	"H" level	0.8 V_{DD}	–	V_{DD}	V
		"L" level	**0**	–	**0.2** V_{DD}	**v**
Input leakage current	I_{IL}	"H" level	–	–	250	μA
		"L" level	-250	–	–	μA
Supply current (Logic)	I_{DD}	Note 3)	–	21	29	mA
Supply currect (LCD dirve)	I_{EE}		–	20	28	mA
Power consumption	Pd		–	450	600	mW

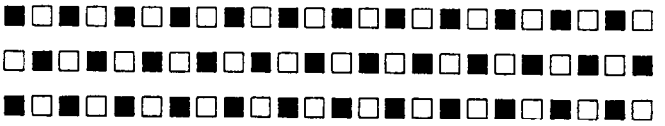
Note 1) The viewing angle θ at which the optimum contrast is obtained by adjusting V_{DD}-V_{EE}. Refer to Fig.4 for the definition of θ.

Note 2) Max. and Min. values are specified as the Max. and Min. voltage within the condition of operational temperature range (0~50 "C). Typ. values are specified as the typical voltage at 25 "C.

Note 3) Display high frequency pattern.

V_{DD} = 3 V, V_{DD} – V_{EE} = 22.0 V, Frame frequency = 85 Hz, Display pattern = 1 bit checker

display pattern



5-2 Input capacitance

Table 5

Signal	Input capacitance
s	40 pF TYP
CP1,DISP	250 pF TYP
CP2	200 pF TYP
DU0~DU3	200 pF TYP
DL0~DL3	200 pF TYP

5-3 Interface signals

Table 6

OLCD

Pin No	Symbo 1	Description	Leve 1
1	S	Scan start-up signal	"H"
2	CP1	Input data latch signal	H→L
3	CP2	Data input clock signal	H→L
4	DISP	Display control signal	Display on ..''H" off. ."L"
5	VDD	Power supply for logic and LCD(+)	
6	Vss	Ground potential	
7	VEE	Power supPlY for LCD (-)	
8	DUO	Display data signal (Upper half)	H(ON),L(OFF)
9	DU 1		
10	DU2		
11	DU3		
12	DLO	Display data signal (Lower half)	H(ON),L(OFF)
13	DL1		
14	DL2		
15	DL3		

○CCFT

Pin No	Symbol	Description	Level
1	GND	Ground line (from Inverter)	
2	NC		
3	NC		
4	HV	High voltage line(from Inverter)	

Note) Pin No, and its location are shown in Fig. 10.

OLCD

Used connector: 53261 -151 O(MOLEX)

Mating connector: 51021 -15 OO(MOLEX)

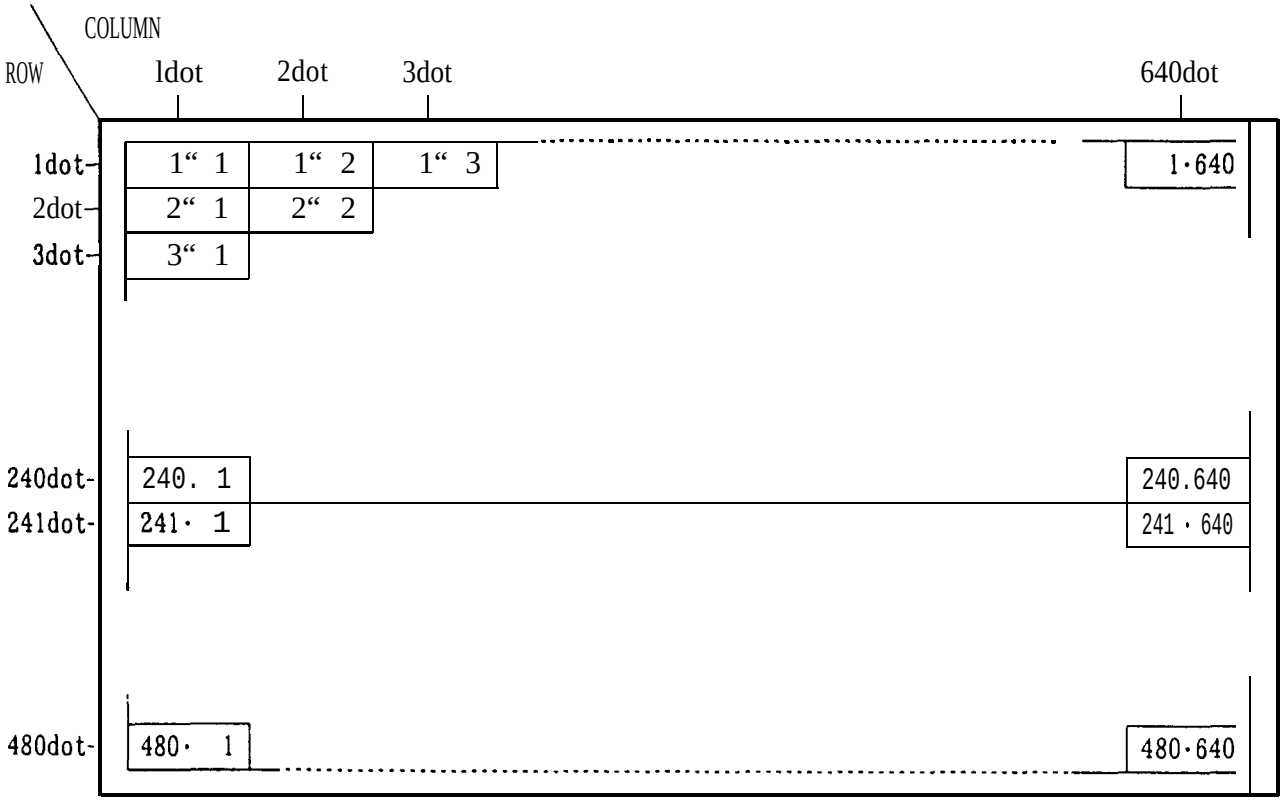
○CCFT

Used connector: M63M83-04(MITSUMI)

Mating connector: M60-04-30-114P(MITSUMI)

M60-04-30-134P(MITSUMI)

M61M73-04(MITSUMI)



Note) 1·2 means 1st row 2nd column dot.

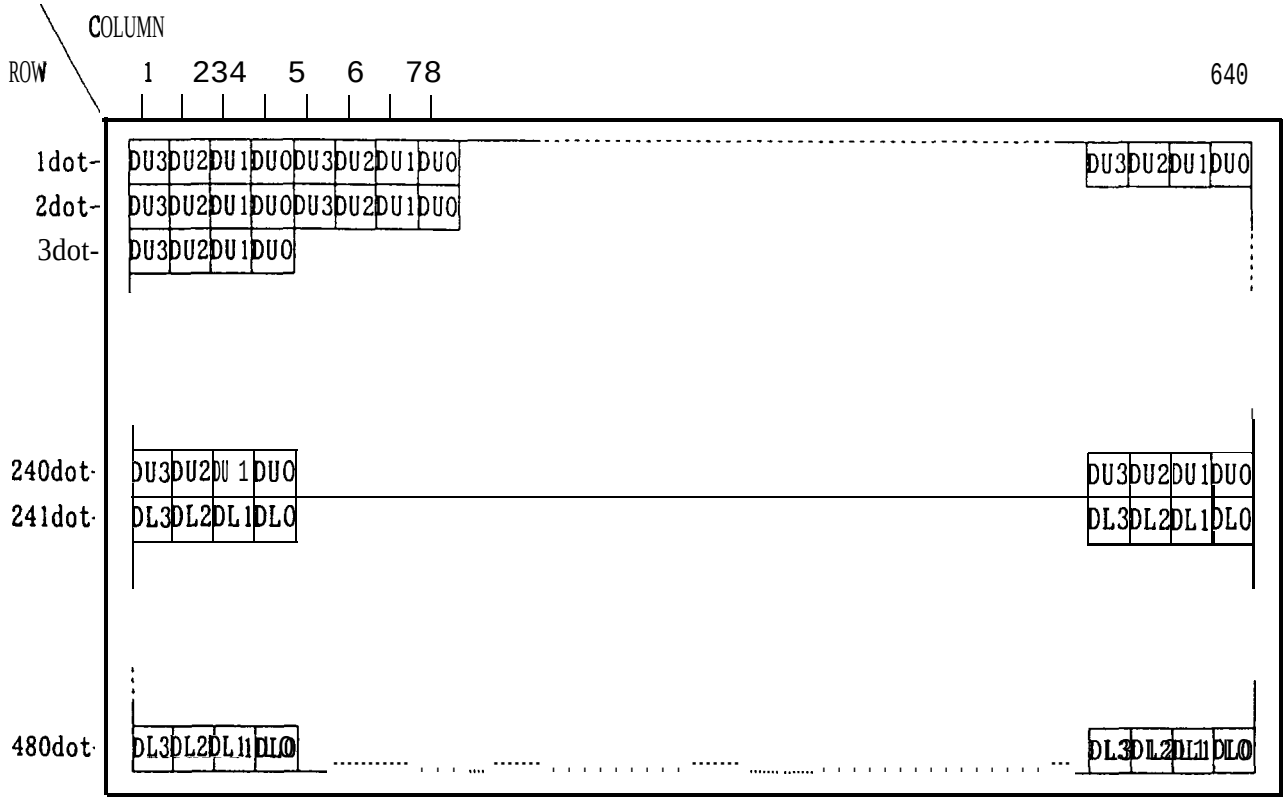


Fig. 1 Dot chart of display area

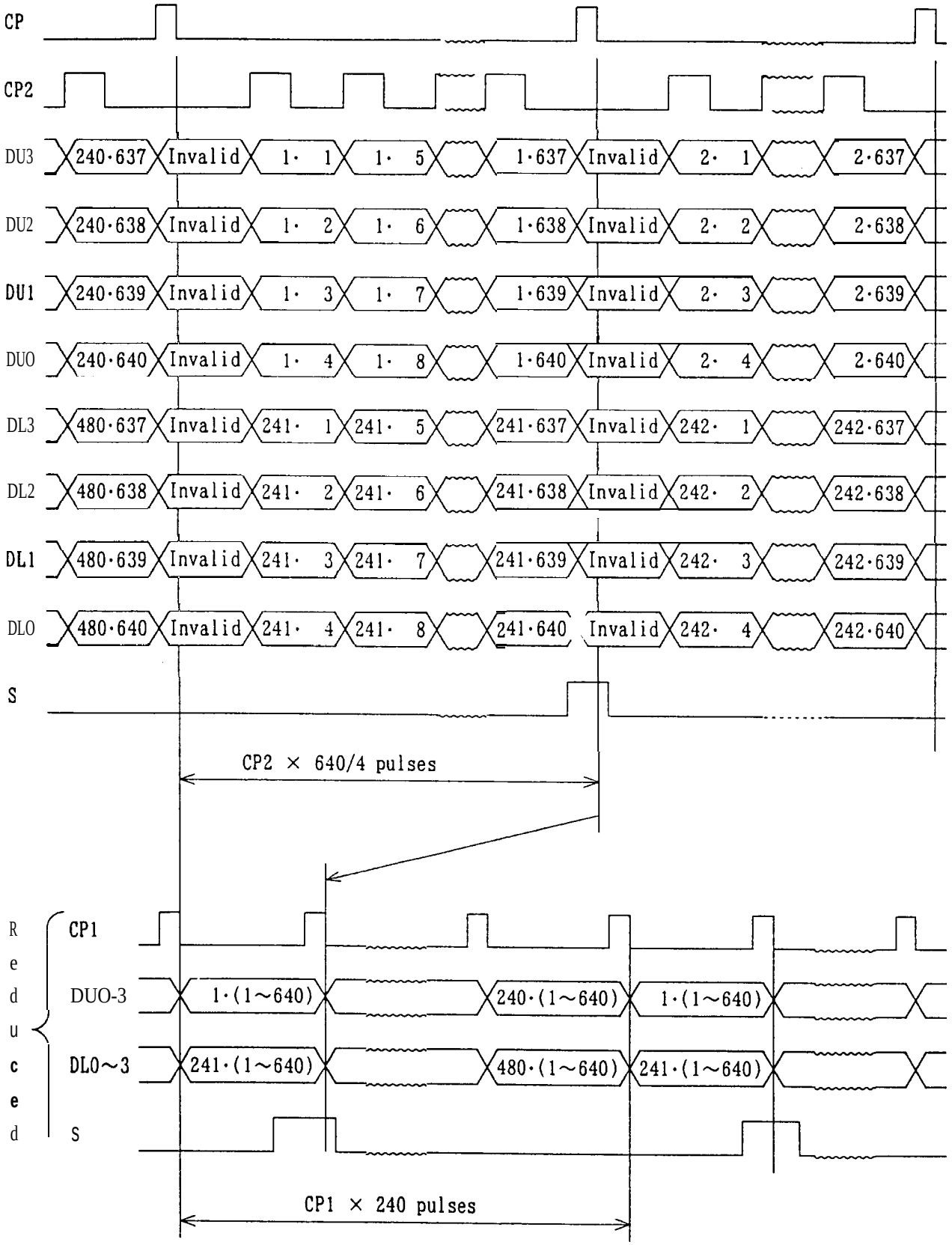
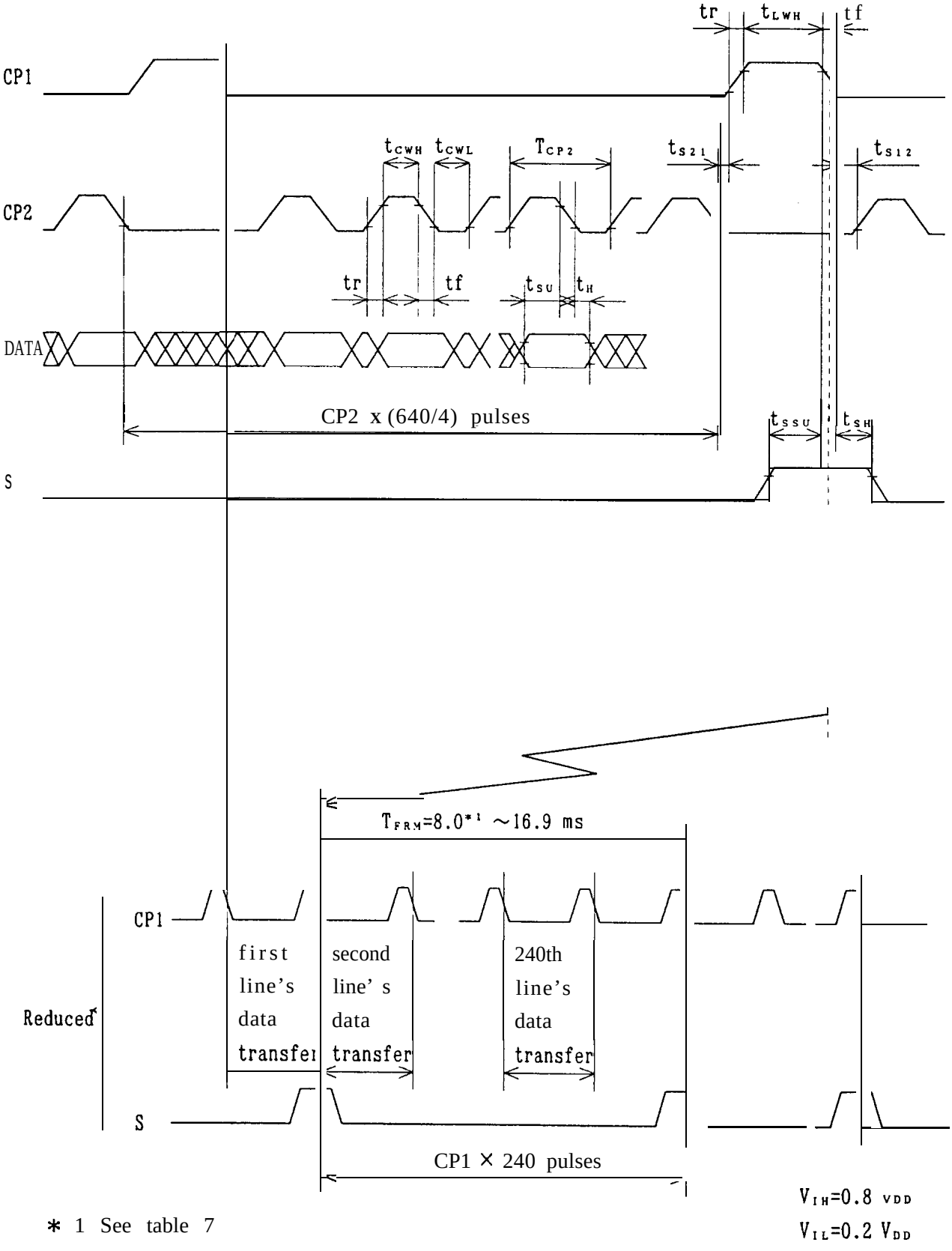


Fig.2 Data input timing



* 1 See table 7

Fig.3 Interface timing chart

Table 7 Interface timing ratings

Item	Symbo 1	Rating			Unit
		MIN.	TYP.	MAX.	
Frame cycle	T_{FRM}	8.0*1		16.9	ms
CP2 clock cycle	T_{CP2}	152			ns
"H" level clock width	t_{CWH}	65			ns
"L" level clock width	t_{CWL}	65			ns
"H" level latch clock width	t_{LWH}	70			ns
Data set up time	t_{SU}	50			ns
Data hold time	t_H	40			ns
S set up time	t_{SSU}	100			ns
S hold time	t_{SH}	100			ns
CP2↑ clock allowance time from CP1↓	t_{s21}	0			ns
CP1↑ clock allowance time from CP2↓	t_{s12}	0			ns
Clock rise/fall time	tr,tf			t_{rf}*2	ns

*1 : LCD Module functions at the minimum frame cycle of 8 ms (Maximum frame frequency of 125Hz). Owing to the characteristics of LCD Module, "shadowing" will become more eminent as frame frequency goes up, while flicker will be reduced.

According to our exper ments, frame cycle of 11.7 ms Min. or frame frequency of 85 Hz Max. w 11 demonstrate optimum display quality in terms of flicker and "shadowing'. But since judgement of display quality is subjective and display quality such as "shadowing" is pattern dependent,it is recommended that decision of frame cycle or frame frequency, to which power consumption of the LCD Module is propotional,be made based on your own through testing on the LCD Module with every possible patterns displayed on it.

*2 : t_{rf} =50 in case $t_{CT}=(T_{CP2}-t_{CWH}-t_{CWL})/2 \geqq 50$

$t_{rf} \square t_{CT}$ in case $t_{CT}=(T_{CP2}-t_{CWH}-t_{CWL})/2 < 50$

6. Module Driving Method

6.1 Circuit configuration

Fig.9 shows the block diagram of the Module's circuitry.

6,2 Display Face Configuration

The display face electrically consists of two (upper and lower) display segments so that the unit may offer higher contrast by reducing drive duty ratio. Each display segment (640x240 dots) is d iven at 1/240 duty ratio.

6.3 Input Data and Control Signal

The LCD driver is 80 bits LSI, cons sting of shift registers, latch circuits and LCD driver circuits.

Display data which are externally divided into data for each row (640dots) will be sequentially transferred in the form of 4-bit parallel data through shift registers by Clock Signal CP2 from the left top of the display face,

When data of one row (640dots) have been input, they will be latched in the form of parallel data for 640 lines of signal electrodes by latch signal CP1. Then the corresponding drive signal will be transmitted to the 640 lines of column electrodes of the LCD panel by the LCD drive circuits,

At this time, scan start-up signal S has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st rows of upper and lower half of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD

While the 1st rows of data are being displayed, the 2nd rows of data are entered When 640 dots of data have been transferred then latched on the falling edge of CP1 clock, the display face proceeds to the 2nd rows of display.

Such data input will be repeated up to the 240th row of each display segment, from upper to lower rows, to complete one frame of display by time sharing method. The data input proceeds to the next display face.

Scan start-up signal S generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction which will deteriorate LCD panel, drive waveform shall be inverted at every display frame to prevent the generation of such DC voltage. Control Signal M plays such role.

Because of the characteristics of the CMOS driver LSI, the power consumption of the Module goes up as the operating frequency CP2 increases. Thus the driver LSI applies the system of transferring 4-bits parallel data through the 4 lines of shift registers to reduce the data transfer speed CP2. Thanks to the LSI, the power consumption of the Module will be minimized.

In this circuit configuration, 4-bit display data shall be therefore input to data input pins of DU_{0-3} (upper display segment) and DL_{0-3} (lower display : egment).

Furthermore the LCD Module adopts bus line system for data input to min mize the power consumption. In this system data input terminal of each driver LSI activated only when relevant data input is fed.

Data input for column electrodes of both the upper and the lower display segment and chip se ect of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the right side is selected when 80 dots data (20CP2) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face.

This process is simultaneously followed at the column drivers LSI's of both the upper and the lower display segments. Thus data input for both the upper and the lower display segments must be fed through 4-bit bus line sequentially from the left end of the display face.

Since this graphic display Module contains no ref esh RAM, it requires data and timing pulse inputs even for static display.

The t ming chart of input signals are shown in Fig. 3 and Table 7.

7. Optical Characteristics Ta=25 ℃, V_{DD}-V_{EE}=Vmax

Table 8

Following spec are based upon the electrical measuring conditions, on which the contrast of perpendicular direction ($\theta x=\theta y=0^{\circ}$) will be MAX.

Parameter		Symbol	Condition		MIN.	TYP.	MAX.	Unit	Remark	
Viewing angle range	Transmissive mode	θx	Co > 2.0	$\theta y=0$ "	-25	-	35	dgr.	Note 1	
		θy		$\theta x=0$ "	-25	-	30	dgr.		
	Reflective mode	θx	Co > 2.0	$\theta y=0$ °	-20	-	35	dgr.		
		θy		$\theta x=0$ °	-25	-	25	dgr.		
Contrast ratio	Transmissive	co	$\theta x=\theta y=0$ "		3 (8)	4.5 (10)	-	-	Note 2	Fig.7-3 Fig.7-1
	Reflective	co	$\theta x=\theta y=0$ °		2.5 (6)	4 (8)	-	-		Fig.7-3 Fig.7-2
Response time	Rise	τr	$\theta x=\theta y=0$ °		-	200	250	ms	Note 3	
	Decay	τd	$\theta x=\theta y=0$ "		-	300	350	ms		

Note 1) The viewing angle range is defined as shown Fig. 4.

Note 2) Contrast ratio is defined as follows:

$$Co=\frac{\text{Luminance(brightness) all pixels "white" at Vmax}}{\text{Luminance(brightness) all pixels "dark" at Vmax}}$$

Vmax is defined in Fig. 6.

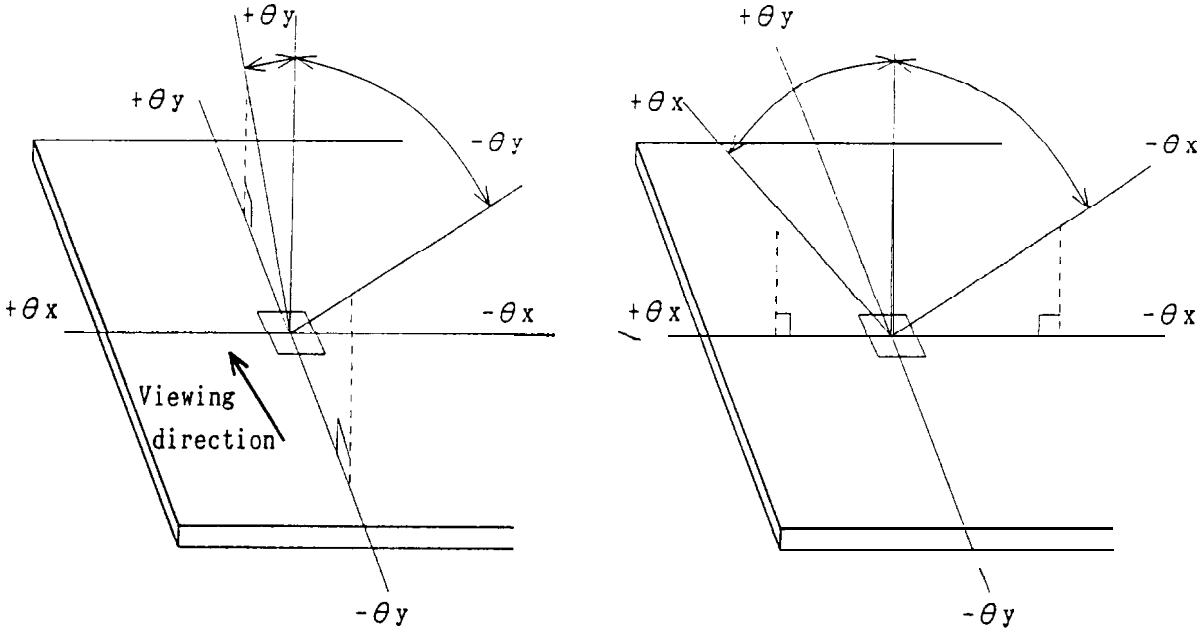
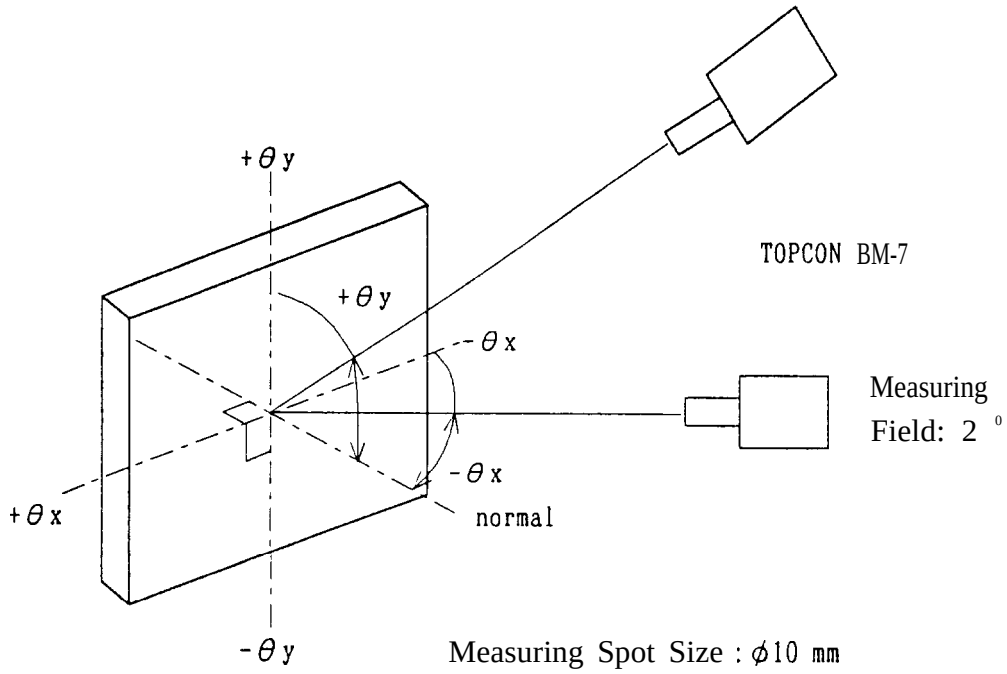


Fig. 4 Definition of Viewing Angle

Note 3) The response characteristics of photo-detector output are measured as shown in Fig.7, assuming that input signals are applied so as to select and deselect the dots to be measured, in the optical characteristics test method shown in Fig.8.



Measuring Spot Size : ϕ10 mm

θx : Angle from "normal"to viewing surface rotated about the horizontal axis,

θy : Angle from "normal"to viewing surface rotated about the vertical axis.

Fig.5 Optical Characteristics Test Method I

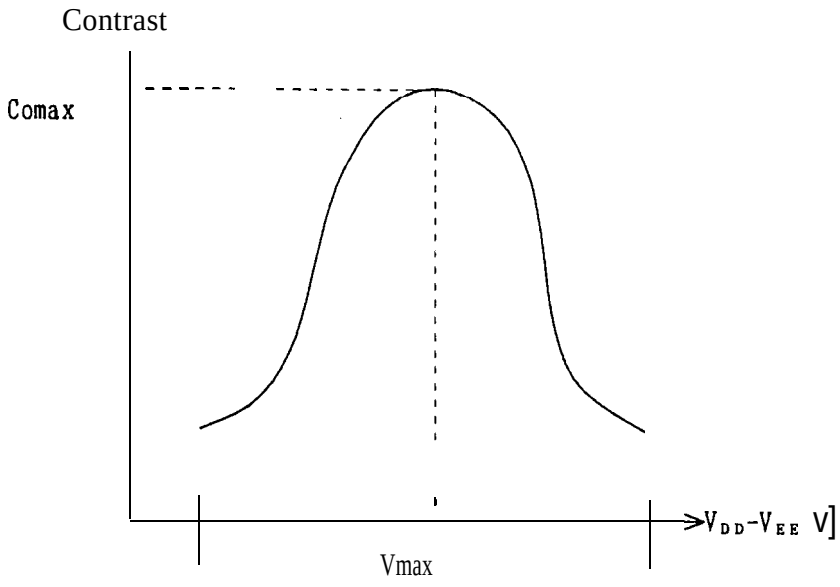


Fig.6 Definition of Vmax

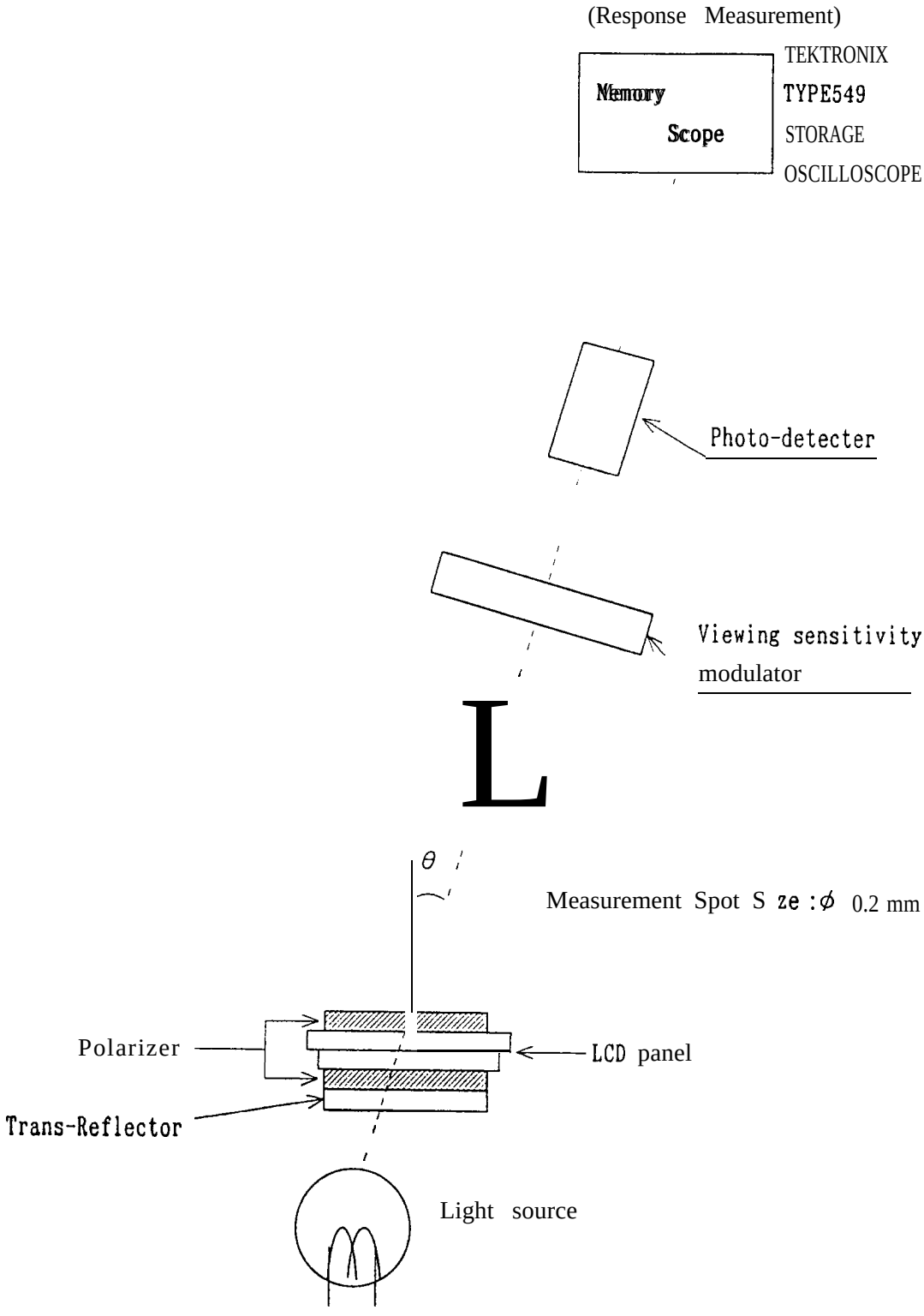


Fig.7-1 Optical Characteristics Test Method 11

(Transmissive mode)

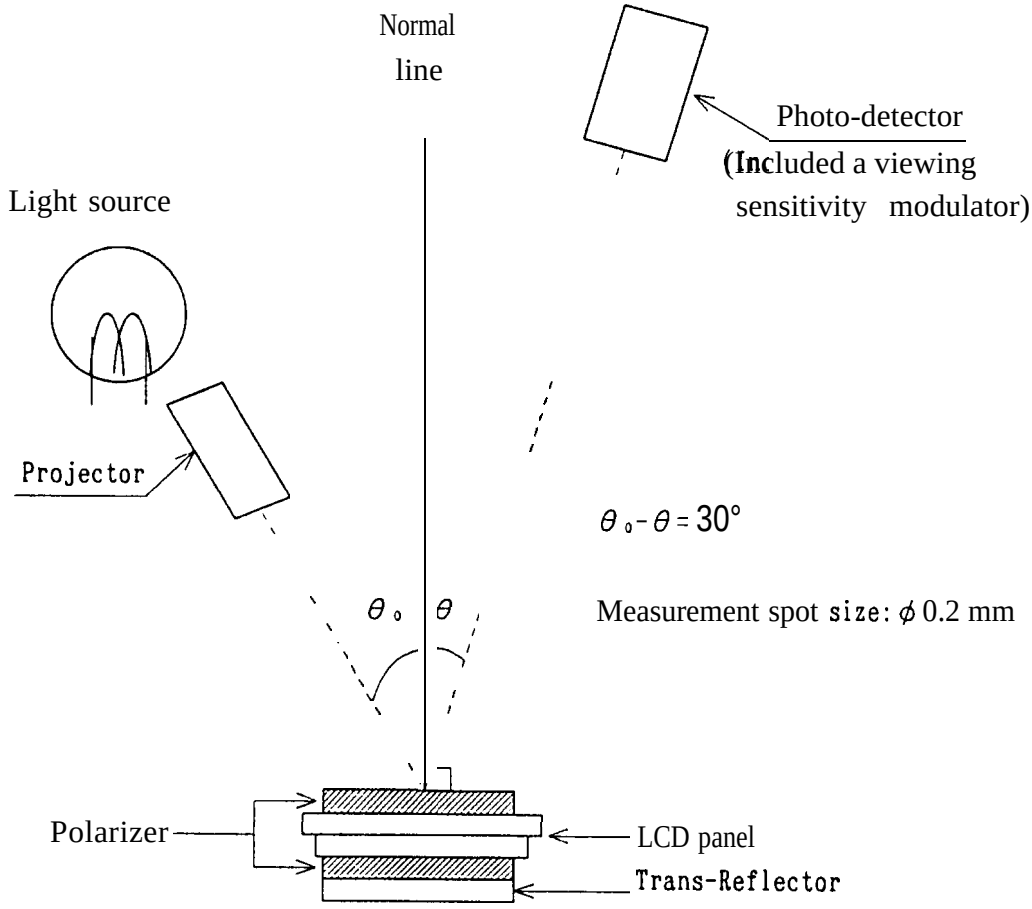
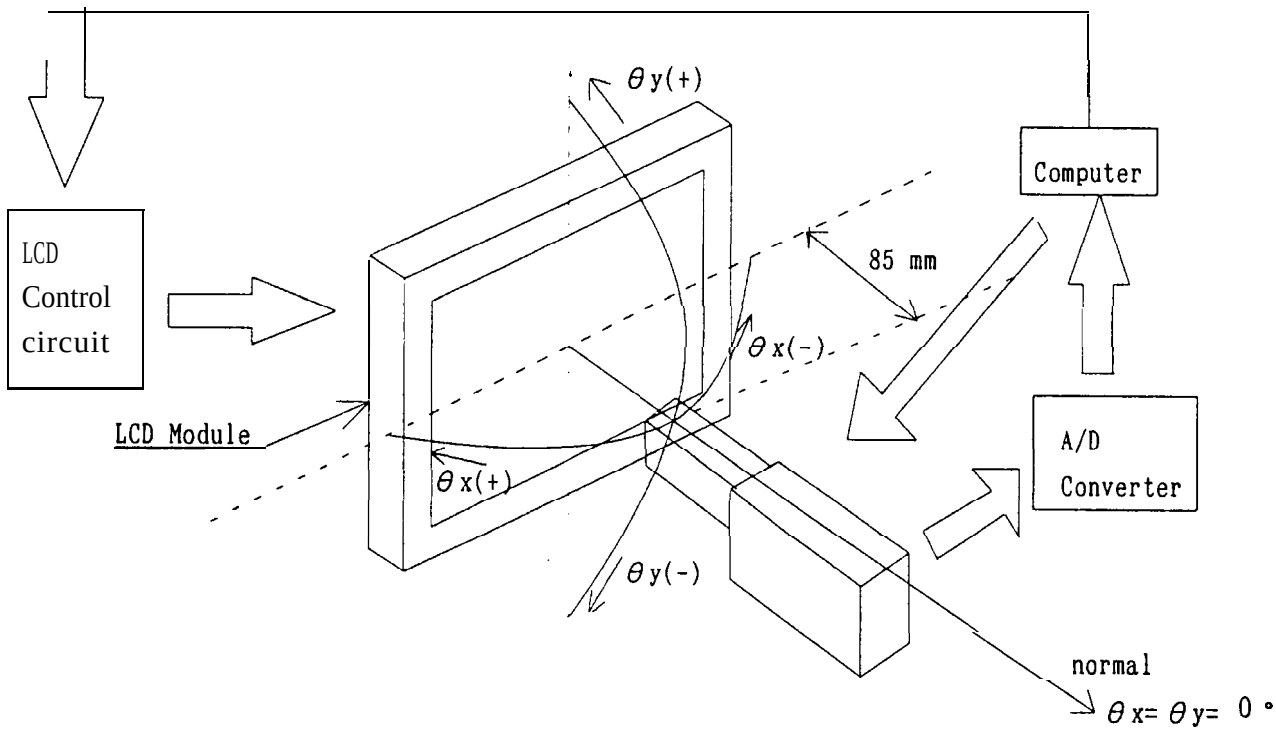


Fig 7-2, Optical Characteristics Test Method III

(Reflective mode)

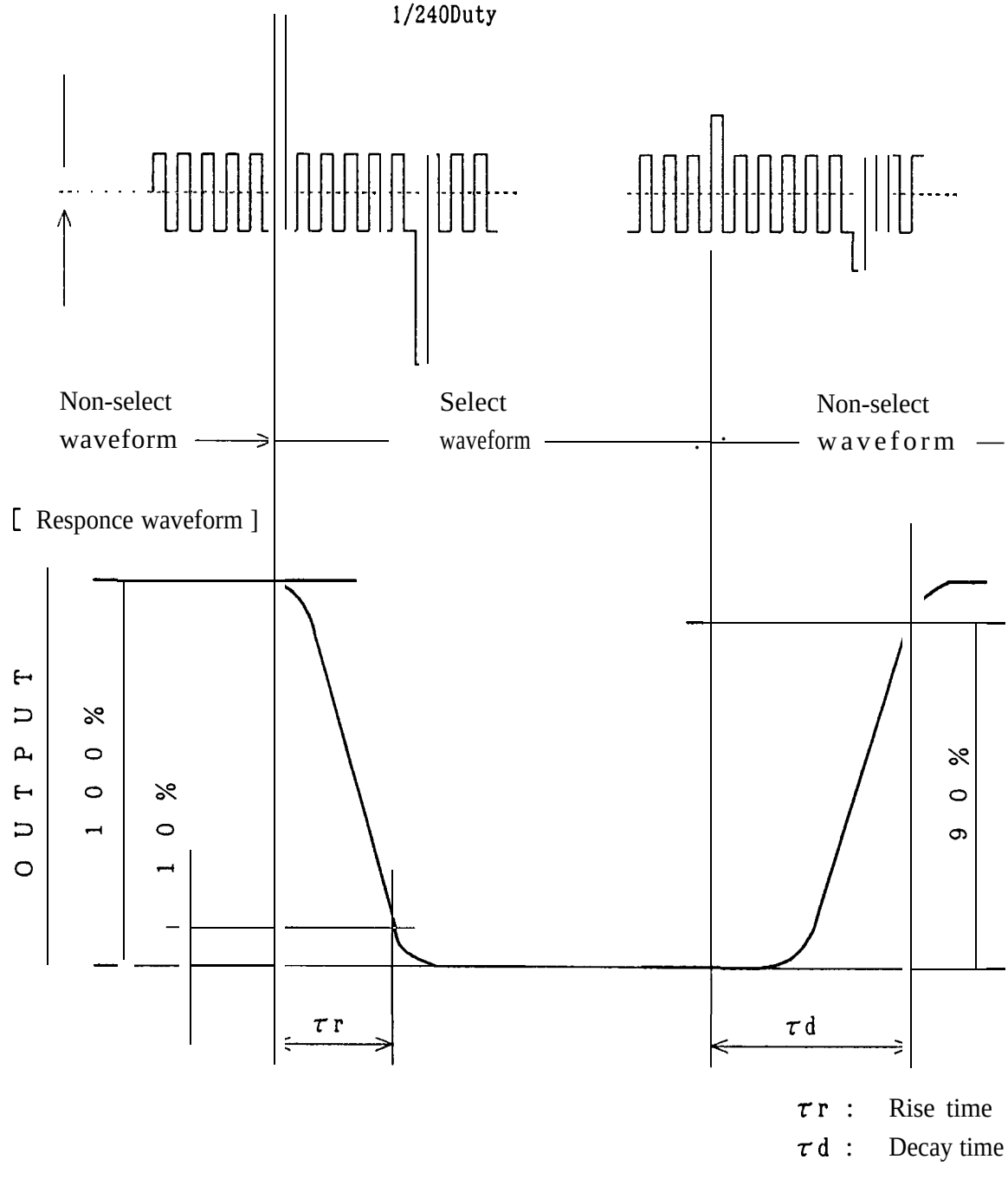
(Response Measurement)
Ta=25 “C
In dark room



TOPCON BM7 + quartz fiber
(Measurirg Spot Size: ϕ 10 mm ,
Measuring Field: 2 “)

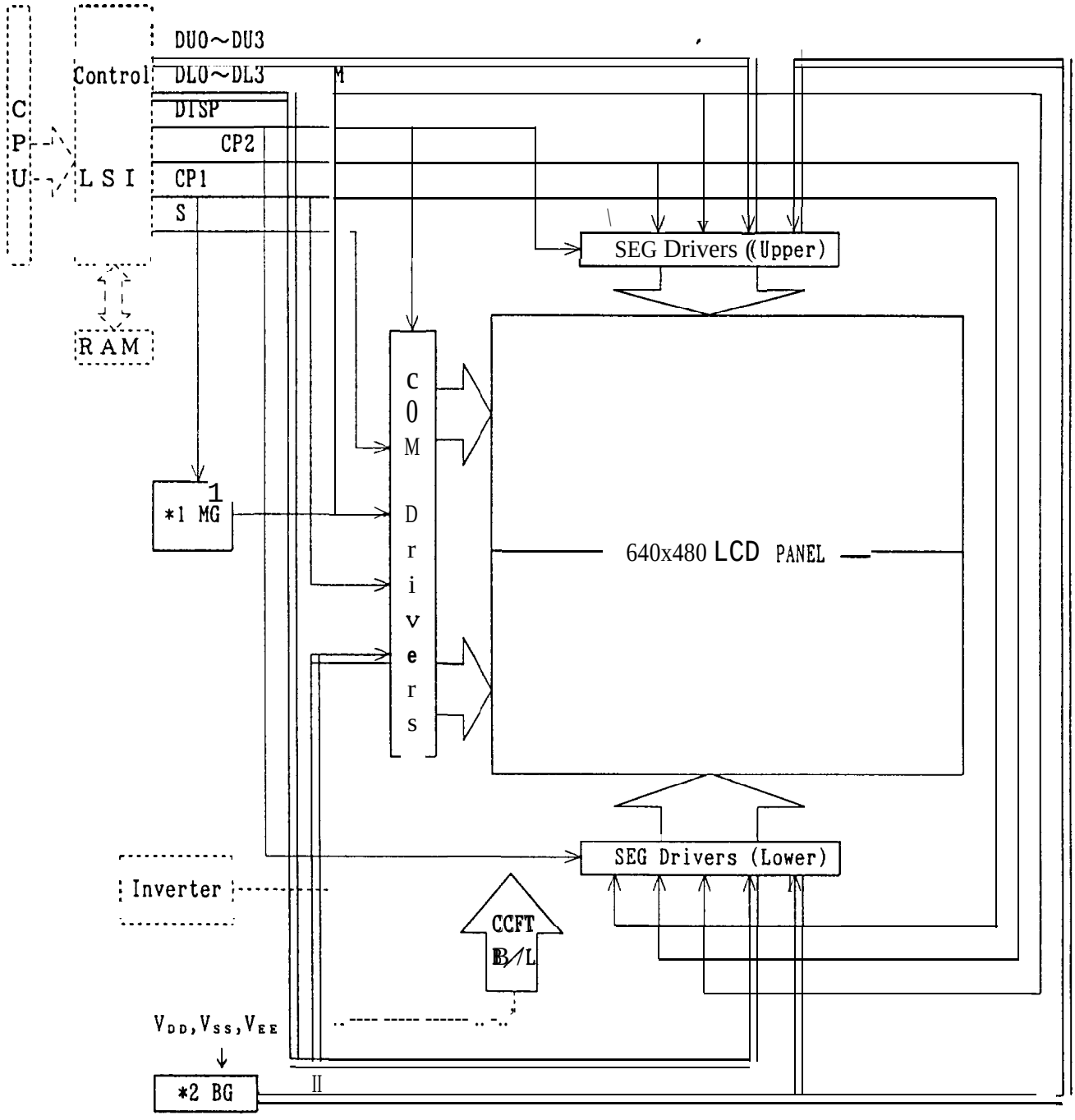
Fig.7-3 Optical Characteristics Test Method IV

[Drive waveform]



τr : Rise time
τd : Decay time

Fig.8 Definition of Response Time



*1 MG: M GENERATOR CIRCUIT
*2 BG: BIAS GENERATOR CIRCUIT

Fig.9 Circuit block diagram

SPEC No.	MODEL No.	PAGE
LC-	LM64K103	9

ISSUE

設計通知 DRAWING INFO. No. ( ) 連絡書 INFORMATION による

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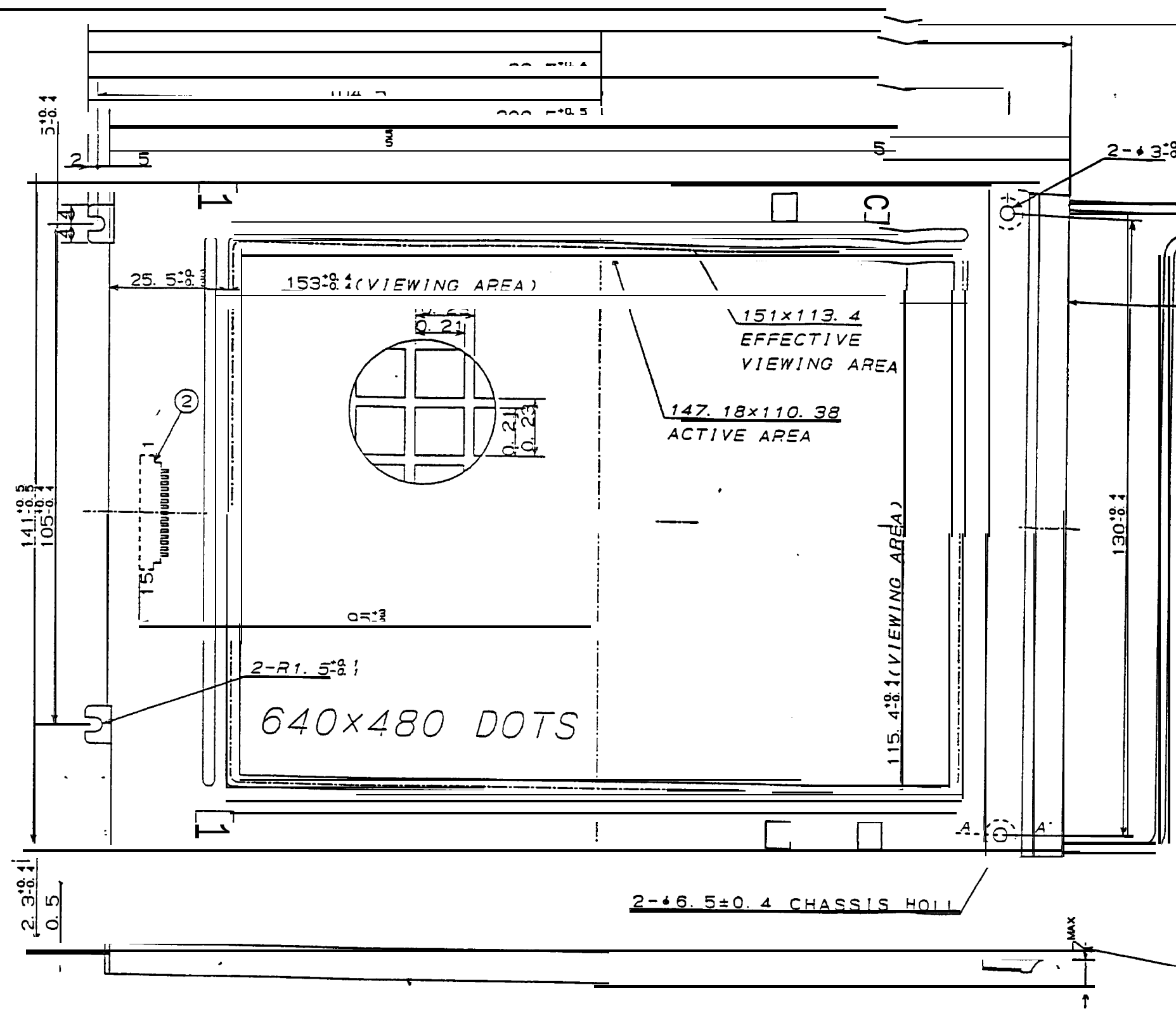

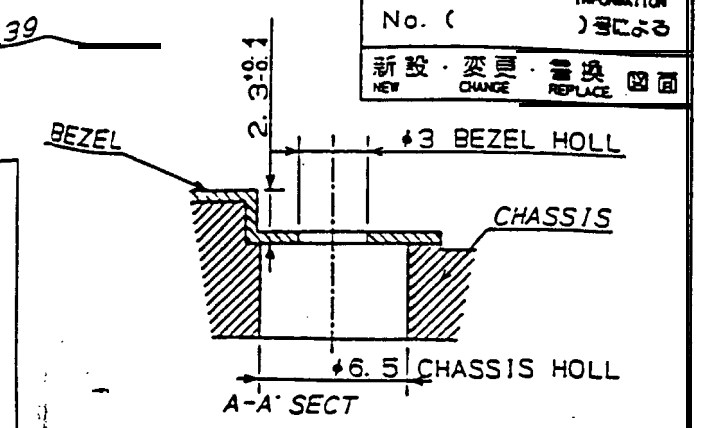

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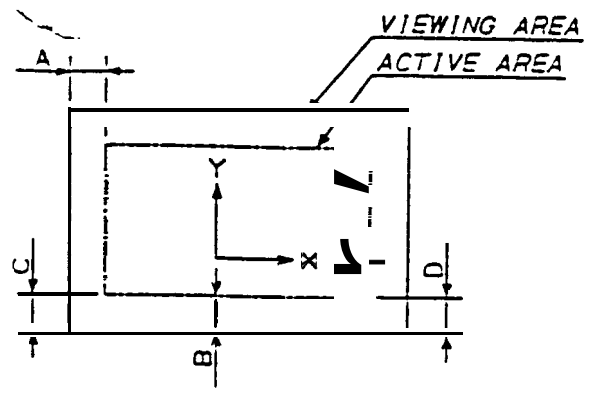

1) TOL(TOLERANCE) X-direction A: 2.91±0.8
2) TOL(TOLERANCE) Y-direction B: 2.51±0.8
3) OBLIQUITY of DISPLAY AREA (C-D)<0.8

① CCFT CONNECTOR
M63M83-04 (MITSUMI)

② INTER FACE CONNECTOR
(15Pins)
53261-1510 (MOLEX)

Excluded the allowance of deformation.

INTER FACE PIN LAYOUT

PIN#	1	2	3	4	5	6	7	8
SYMBOL	S	CP1	CP2	DISP OFF	VDD	VSS	VEE	DUO
PIN#	9	10	11	12	13	14	15	
SYMBOL	DU1	DU2	DU3	DL0	DL1	DL2	DL3	

指示なき寸法公差は UNSPECIFIED TOL TO BE

V1 2	年月日 DATE	改定記事 REVISED	担当	LM64K103 適用機種 DEL	名称 NAME	LCD UNIT OUTLINE DIMENSION	
MATERIAL	THICKNESS	FINISH	—	SCALE	記号 SYMBOL		
設計 DESIGN	製図 TRACE	検図 CHECK	検図 CHECK	承認 APPROVE	製品コード PARTS CODE		
				SHARP CORPORATION シャープ株式会社 双葉(事本) デュータイ開発セン	作成日付 DATE	1996・2・21・	